



# VND5N07/VND5N07-1 VNP5N07FI/K5N07FM

"OMNIFET":  
FULLY AUTOPROTECTED POWER MOSFET

**Table 1. General Features**

Type	V <sub>clamp</sub>	R <sub>DS(on)</sub>	I <sub>lim</sub>
VND5N07 VND5N07-1 VND5N07FI VND5N07FM	70 V	0.2 Ω	5 A

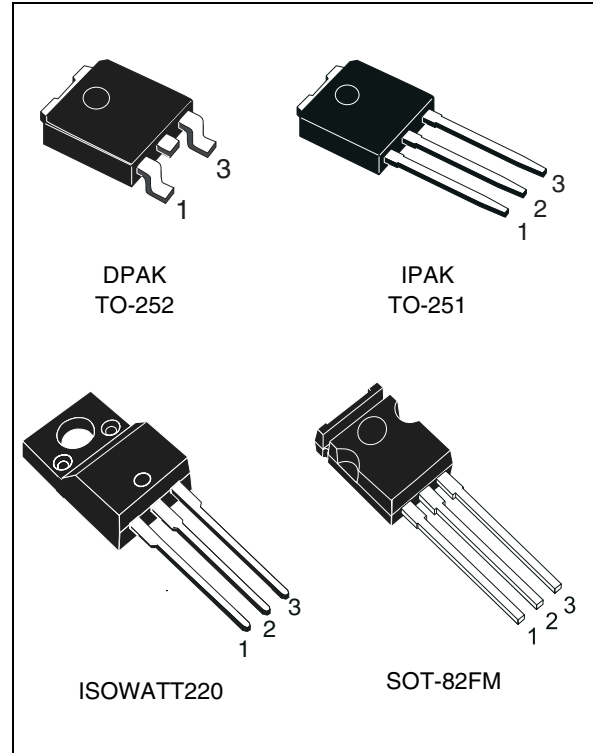
- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

## DESCRIPTION

The VND5N07, VND5N07-1, VNP5N07FI and VNK5N07FM are monolithic devices made using STMicroelectronics VIPower M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shut-down, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

**Figure 1. Package**



**Table 2. Order Codes**

Package	Tube	Tape and Reel
DPAK	VND5N07	VND5N0713TR
IPAK	VND5N07-1	—
ISOWATT220	VND5N07FI	—
SOT-82FM	VND5N07FM	—

Figure 2. Block Diagram

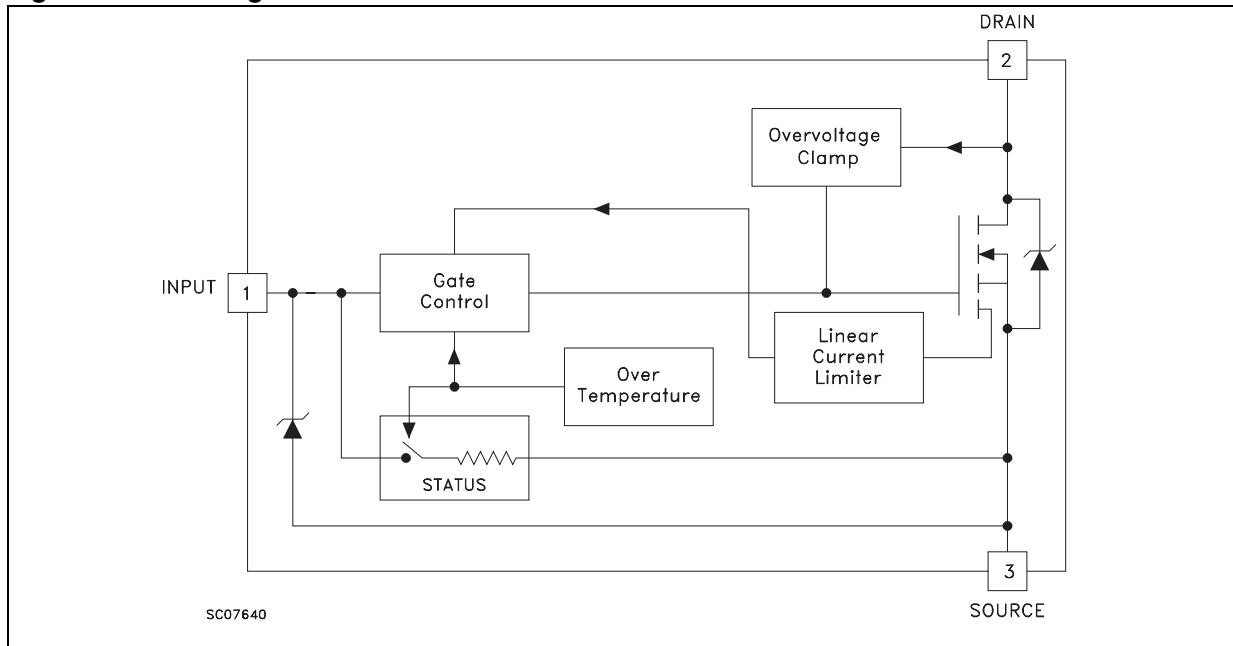


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value			Unit
		DPAK IPAK	ISOWATT220	SOT-82FM	
$V_{DS}$	Drain-Source Voltage ( $V_{in} = 0$ )	Internally Clamped			V
$V_{in}$	Input Voltage	18			V
$I_D$	Drain Current	Internally Limited			A
$I_R$	Reverse DC Output Current	-7			A
$V_{esd}$	Electrostatic Discharge ( $C = 100$ pF, $R = 1.5$ K $\Omega$ )	2000			V
$P_{tot}$	Total Dissipation at $T_c = 25$ °C	60	24	9	W
$T_j$	Operating Junction Temperature	Internally Limited			°C
$T_c$	Case Operating Temperature	Internally Limited			°C
$T_{stg}$	Storage Temperature	-55 to 150			°C

Table 4. Thermal Data

Symbol	Parameter	DPAK/IPAK	ISOWATT220	SOT-82FM	Unit
$R_{thj-case}$	Thermal Resistance Junction-case Max	3.75	5.2	14	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	100	62.5	100	°C/W

**ELECTRICAL CHARACTERISTICS** ( $T_{\text{case}} = 25^{\circ}\text{C}$  unless otherwise specified)**Table 5. Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{CLAMP}}$	Drain-source Clamp Voltage	$I_{\text{D}} = 200 \text{ mA}; V_{\text{in}} = 0$	60	70	80	V
$V_{\text{CLTH}}$	Drain-source Threshold Voltage	$I_{\text{D}} = 2 \text{ mA}; V_{\text{in}} = 0$	55			V
$V_{\text{INCL}}$	Input-Source Reverse Clamp Voltage	$I_{\text{in}} = -1 \text{ mA}$	-1		-0.3	V
$I_{\text{DSS}}$	Zero Input Voltage Drain Current ( $V_{\text{in}} = 0$ )	$V_{\text{DS}} = 13 \text{ V}; V_{\text{in}} = 0$ $V_{\text{DS}} = 25 \text{ V}; V_{\text{in}} = 0$			50 200	$\mu\text{A}$ $\mu\text{A}$
$I_{\text{ISS}}$	Supply Current from Input Pin	$V_{\text{DS}} = 0 \text{ V}; V_{\text{in}} = 10 \text{ V}$		250	500	$\mu\text{A}$

**Table 6. On** <sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{IN(th)}}$	Input Threshold Voltage	$V_{\text{DS}} = V_{\text{in}}; I_{\text{D}} + I_{\text{in}} = 1 \text{ mA}$	0.8		3	V
$R_{\text{DS(on)}}$	Static Drain-source On Resistance	$V_{\text{in}} = 10 \text{ V}; I_{\text{D}} = 2.5 \text{ A}$ $V_{\text{in}} = 5 \text{ V}; I_{\text{D}} = 2.5 \text{ A}$			0.200 0.280	$\Omega$ $\Omega$

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 7. Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{\text{fs}}$ <sup>(2)</sup>	Forward Transconductance	$V_{\text{DS}} = 13 \text{ V}; I_{\text{D}} = 2.5 \text{ A}$	3	4		S
$C_{\text{oss}}$	Output Capacitance	$V_{\text{DS}} = 13 \text{ V}; f = 1 \text{ MHz}; V_{\text{in}} = 0$		200	300	pF

Note: 2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

**Table 8. Switching** <sup>(3)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DD}} = 15 \text{ V}; I_{\text{d}} = 2.5 \text{ A};$		50	100	ns
$t_{\text{r}}$	Rise Time	$V_{\text{gen}} = 10\text{V}; R_{\text{gen}} = 10 \Omega$		60	100	ns
$t_{\text{d(off)}}$	Turn-off Delay Time	(see Figure 28)		150	300	ns
$t_{\text{f}}$	Fall Time			40	80	ns
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DD}} = 15 \text{ V}; I_{\text{d}} = 2.5 \text{ A};$		150	250	ns
$t_{\text{r}}$	Rise Time	$V_{\text{gen}} = 10\text{V}; R_{\text{gen}} = 1000 \Omega$		400	600	ns
$t_{\text{d(off)}}$	Turn-off Delay Time	(see Figure 28)		3900	5000	ns
$t_{\text{f}}$	Fall Time			1100	1600	ns
$(di/dt)_{\text{on}}$	Turn-on Current Slope	$V_{\text{DD}} = 15 \text{ V}; I_{\text{D}} = 2.5 \text{ A}$ $V_{\text{in}} = 10 \text{ V}; R_{\text{gen}} = 10 \Omega$		80		A/ $\mu\text{S}$
$Q_{\text{i}}$	Total Input Charge	$V_{\text{DD}} = 12 \text{ V}; I_{\text{D}} = 2.5 \text{ A}; V_{\text{in}} = 10 \text{ V}$		18		nC

Note: 3. Parameters guaranteed by design/characterization.

**ELECTRICAL CHARACTERISTICS** (cont'd)

**Table 9. Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(4)}$	Forward On Voltage	$I_{SD} = 2.5 \text{ A}; V_{in} = 0$			1.6	V
$t_{rr}^{(5)}$	Reverse Recovery Time	$I_{SD} = 2.5 \text{ A}; di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 30 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$ (see test circuit, Figure 30)		150		ns
$Q_{rr}^{(5)}$	Reverse Recovery Charge			0.3		$\mu\text{C}$
$I_{RRM}^{(5)}$	Reverse Recovery Current			5.7		A

Note: 4. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%  
5. Parameters guaranteed by design/characterization.

**Table 10. Protection**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{lim}$	Drain Current Limit	$V_{in} = 10 \text{ V}; V_{DS} = 13 \text{ V}$ $V_{in} = 5 \text{ V}; V_{DS} = 13 \text{ V}$	3.5 3.5	5 5	7 7	A A
$t_{dim}^{(6)}$	Step Response Current Limit	$V_{in} = 10 \text{ V}$ $V_{in} = 5 \text{ V}$		15 40	20 60	$\mu\text{s}$ $\mu\text{s}$
$T_{jsh}^{(6)}$	Overtemperature Shutdown		150			$^\circ\text{C}$
$T_{jrs}^{(6)}$	Overtemperature Reset		135			$^\circ\text{C}$
$I_{gf}^{(6)}$	Fault Sink Current	$V_{in} = 10 \text{ V}; V_{DS} = 13 \text{ V}$ $V_{in} = 5 \text{ V}; V_{DS} = 13 \text{ V}$		50 20		mA mA
$E_{as}^{(6)}$	Single Pulse Avalanche Energy	starting $T_J = 25 \text{ }^\circ\text{C}; V_{DD} = 20 \text{ V}$ $V_{in} = 10 \text{ V}; R_{gen} = 1 \text{ K}\Omega; L = 10 \text{ mH}$	0.2			J

Note: 6. Parameters guaranteed by design/characterization.

**PROTECTION FEATURES**

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user’s standpoint is that a small DC current ( $I_{ISS}$ ) flows into the Input pin in order to supply the internal circuitry.

The device integrates:

- **OVERVOLTAGE CLAMP PROTECTION:** internally set at 70V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- **LINEAR CURRENT LIMITER CIRCUIT:** limits the drain current  $I_d$  to  $I_{lim}$  whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, and the ability to be driven from a TTL Logic circuit

junction temperature may reach the overtemperature threshold  $T_{jsh}$ .

- **OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:** these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150 $^\circ\text{C}$ . The device is automatically restarted when the chip temperature falls below 135 $^\circ\text{C}$ .
- **STATUS FEEDBACK:** In the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100  $\Omega$ . The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model (with a small increase in  $R_{DS(on)}$ ).



Figure 3. Thermal Impedance for DPAK/IPAK

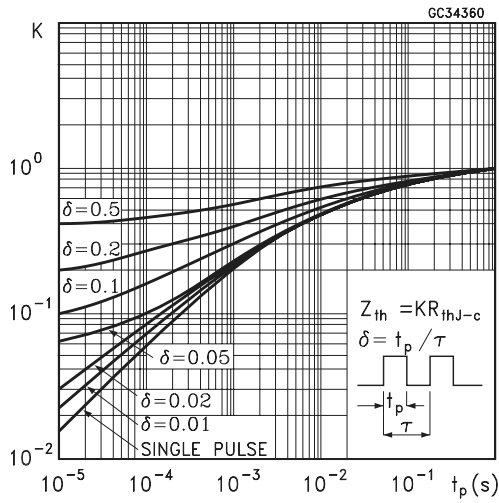


Figure 4. Thermal Impedance for ISOWATT220

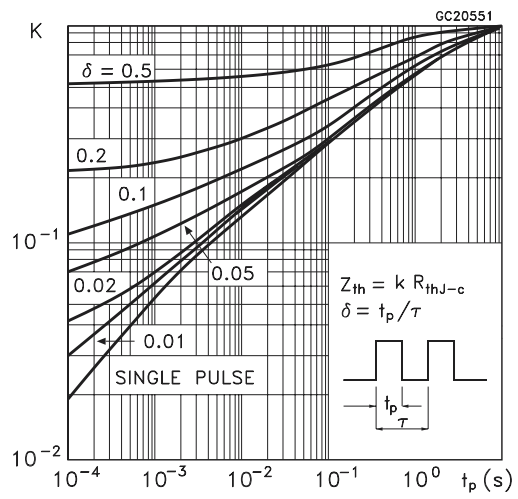


Figure 5. Derating Curve

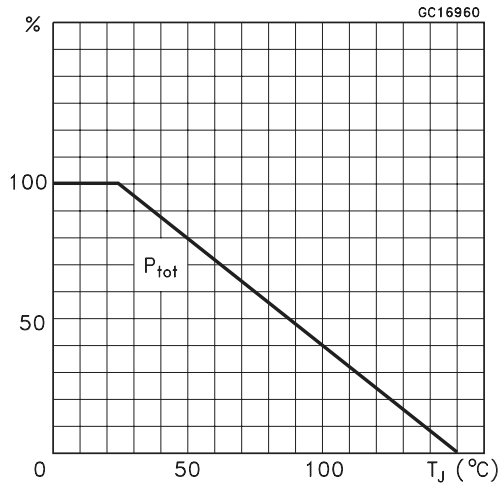


Figure 6. Output Characteristics

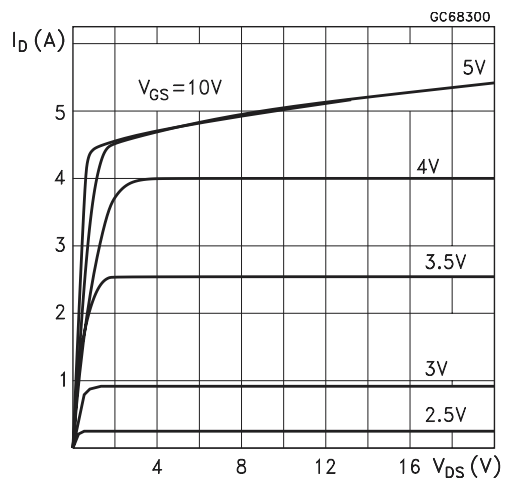


Figure 7. Transconductance

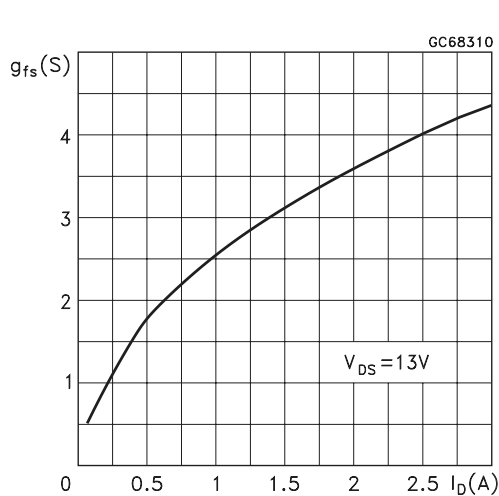


Figure 8. Static Drain-source On Resistance vs Input Voltage

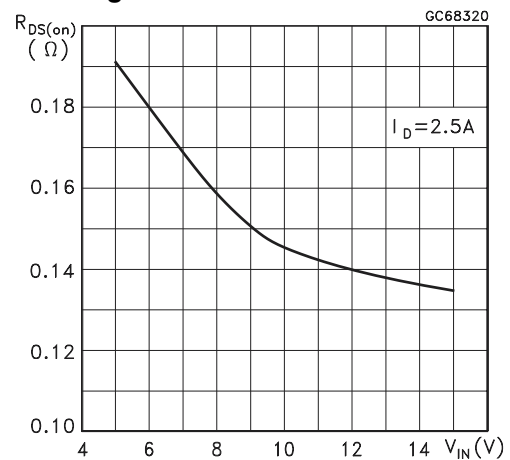


Figure 9. Static Drain-Source On Resistance

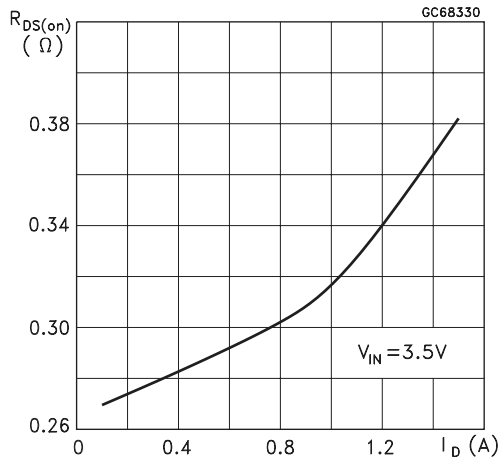


Figure 10. Static Drain-Source On Resistance

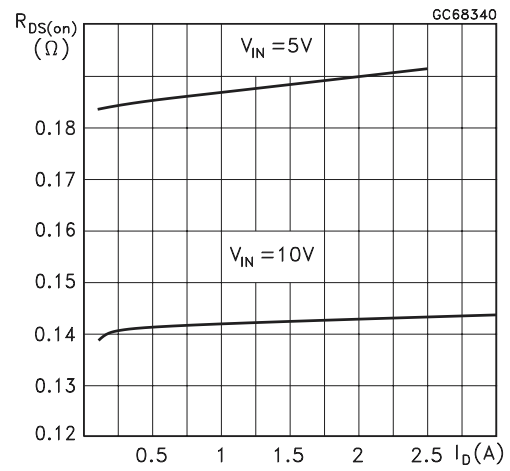


Figure 11. Input Charge vs Input Voltage

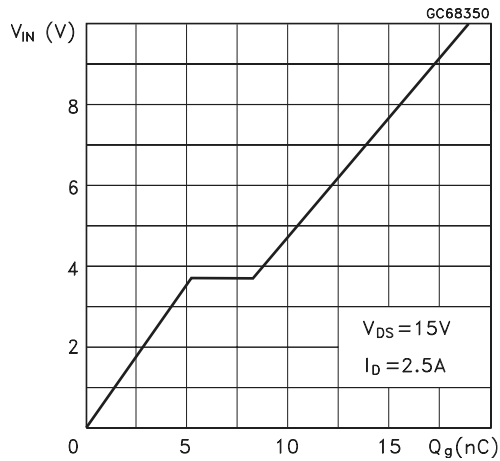


Figure 12. Capacitance Variations

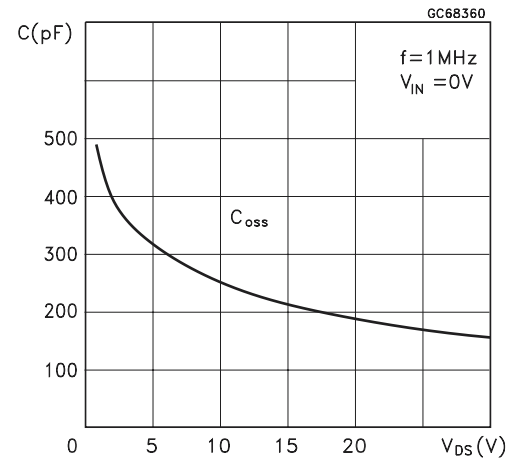


Figure 13. Normalized Input Threshold Voltage vs Temperature

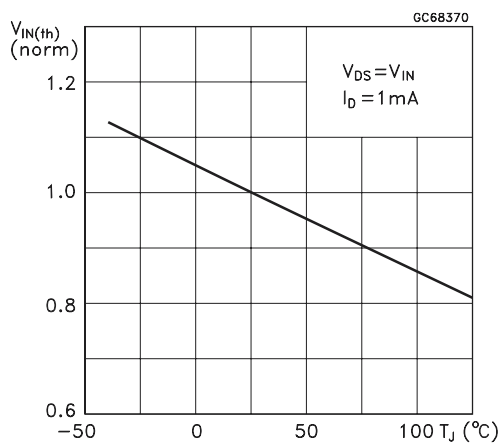


Figure 14. Normalized On Resistance vs Temperature

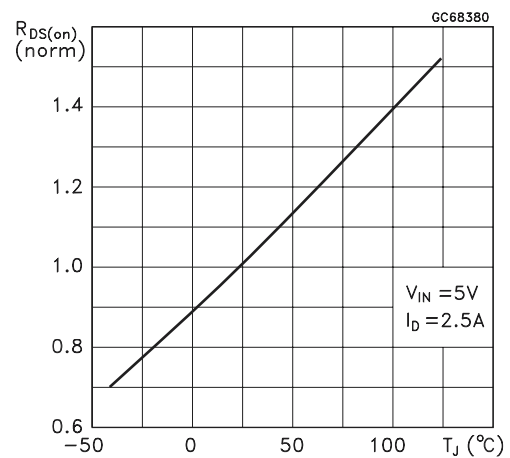


Figure 15. Normalized On Resistance vs Temperature

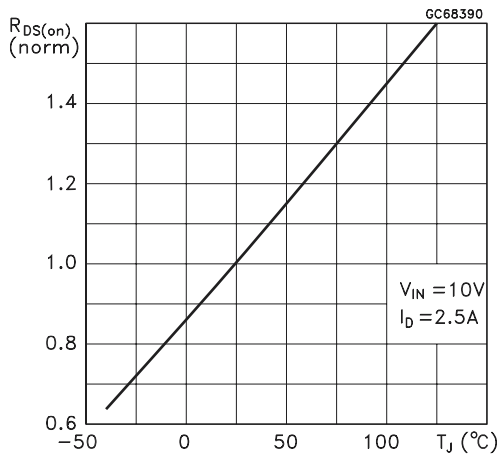


Figure 16. Turn-on Current Slope

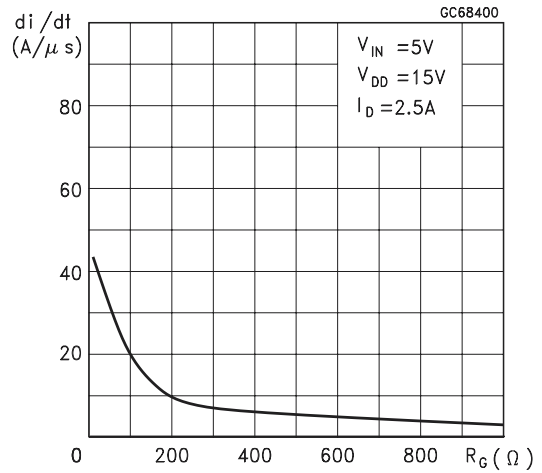


Figure 17. Turn-on Current Slope

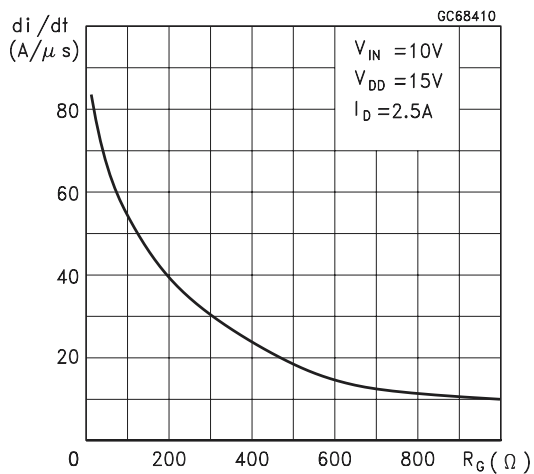


Figure 18. Turn-off Drain-Source Voltage Slope

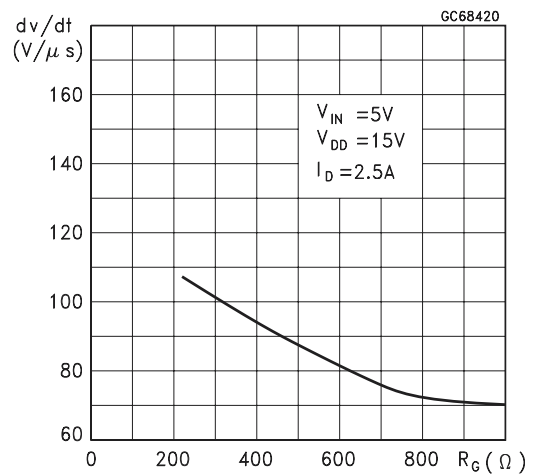


Figure 19. Turn-off Drain-Source Voltage Slope

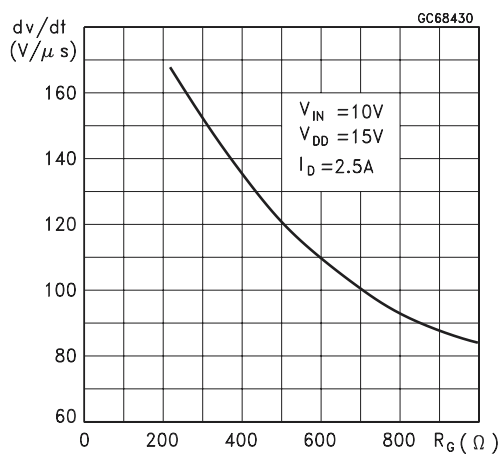


Figure 20. Switching Time Resistive Load

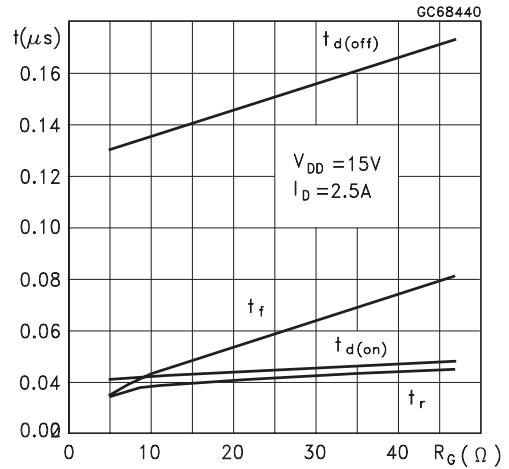


Figure 21. Switching Time Resistive Load

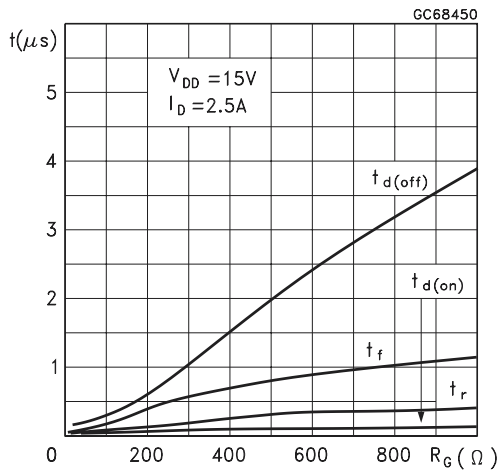


Figure 22. Switching Time Resistive Load

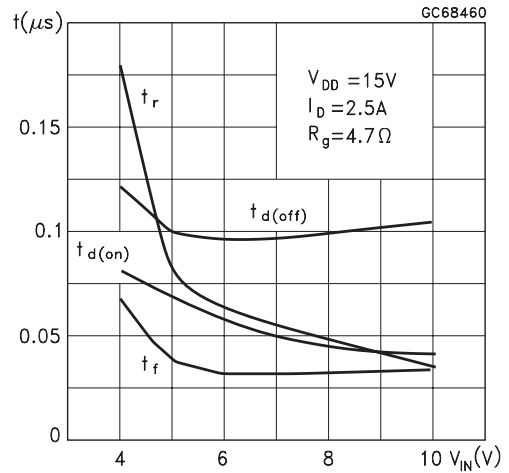


Figure 23. Current Limit vs Junction Temperature

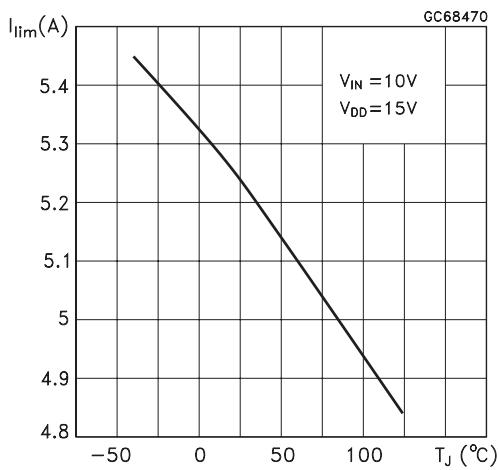


Figure 24. Step Response Current Limit

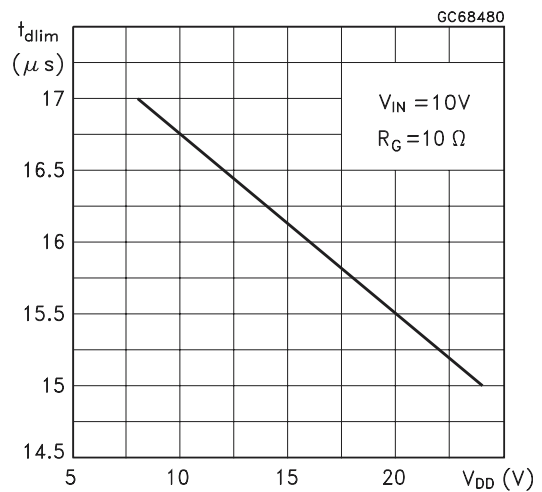


Figure 25. Source Drain Diode Forward Characteristics

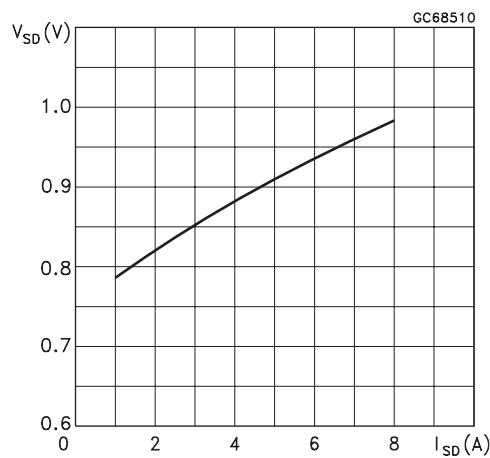




Figure 26. Unclamped Inductive Load Test Circuit

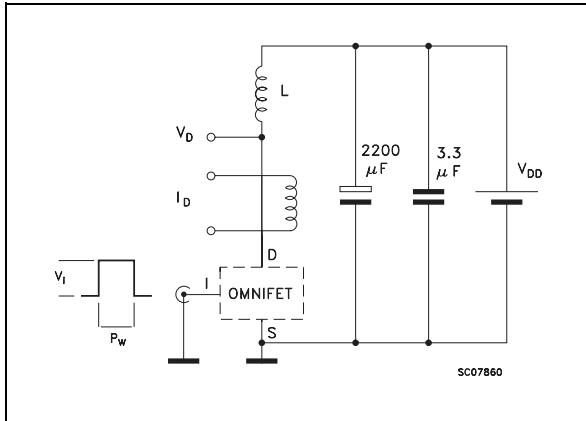


Figure 27. Unclamped Inductive Waveforms

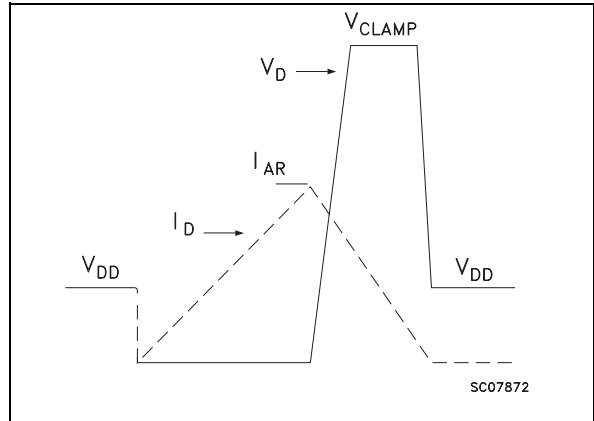


Figure 28. Switching Times Test Circuits For Resistive Load

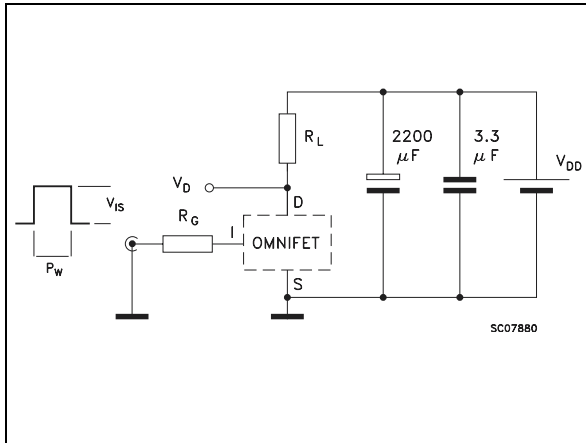


Figure 29. Input Charge Test Circuit

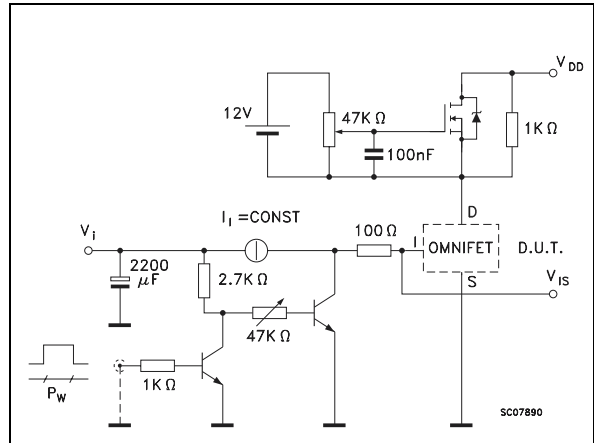


Figure 30. Test Circuit For Inductive Load Switching And Diode Recovery Times

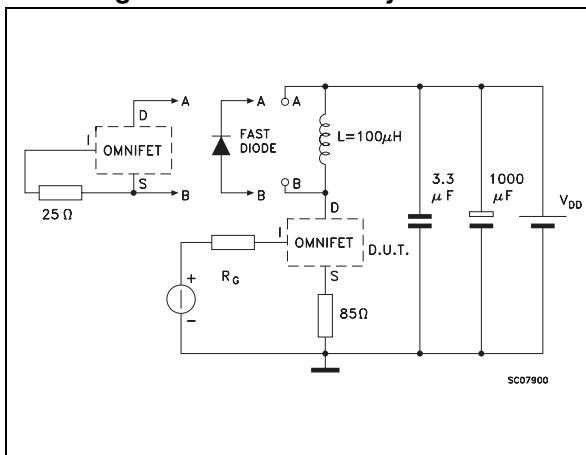
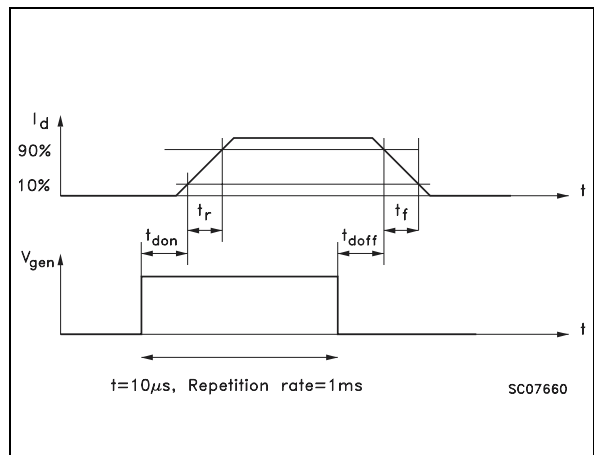


Figure 31. Waveforms

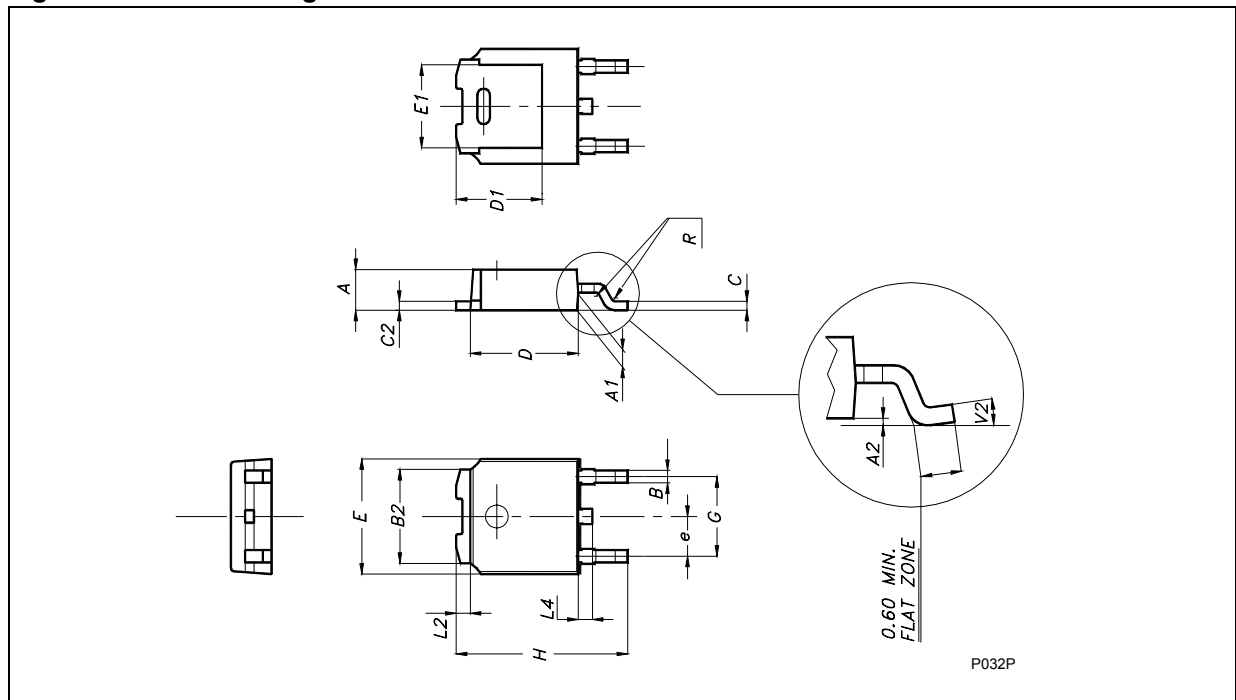


PACKAGE MECHANICAL

Table 11. DPAK Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package Weight	Gr. 0.29		

Figure 32. DPAK Package Dimensions

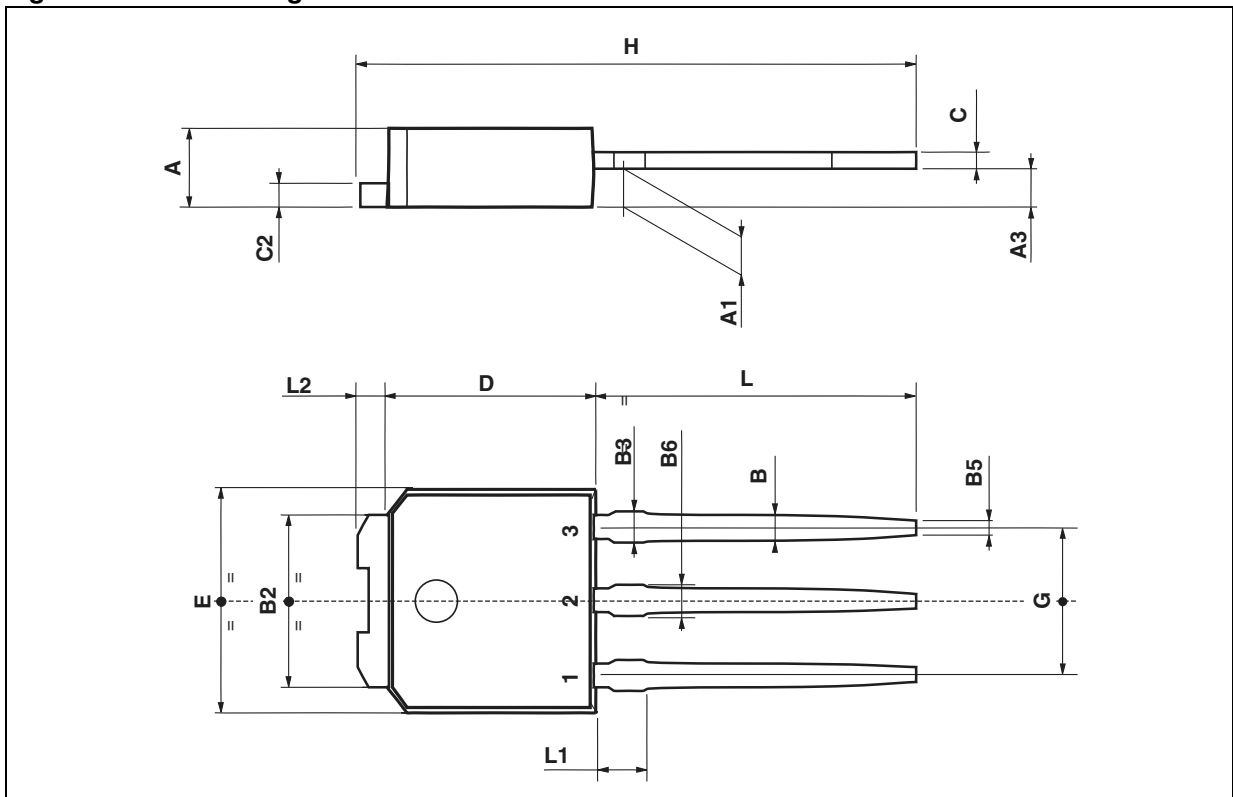


Note: Drawing is not to scale.

Table 12. IPAK Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.2		2.4
A1	0.9		1.1
A3	0.7		1.3
B	0.64		0.9
B2	5.2		5.4
B3			0.85
B5		0.3	
B6			0.95
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
E	6.4		6.6
G	4.4		4.6
H	15.9		16.3
L	9		9.4
L1	0.8		1.2
L2		0.8	1

Figure 33. IPAK Package Dimensions



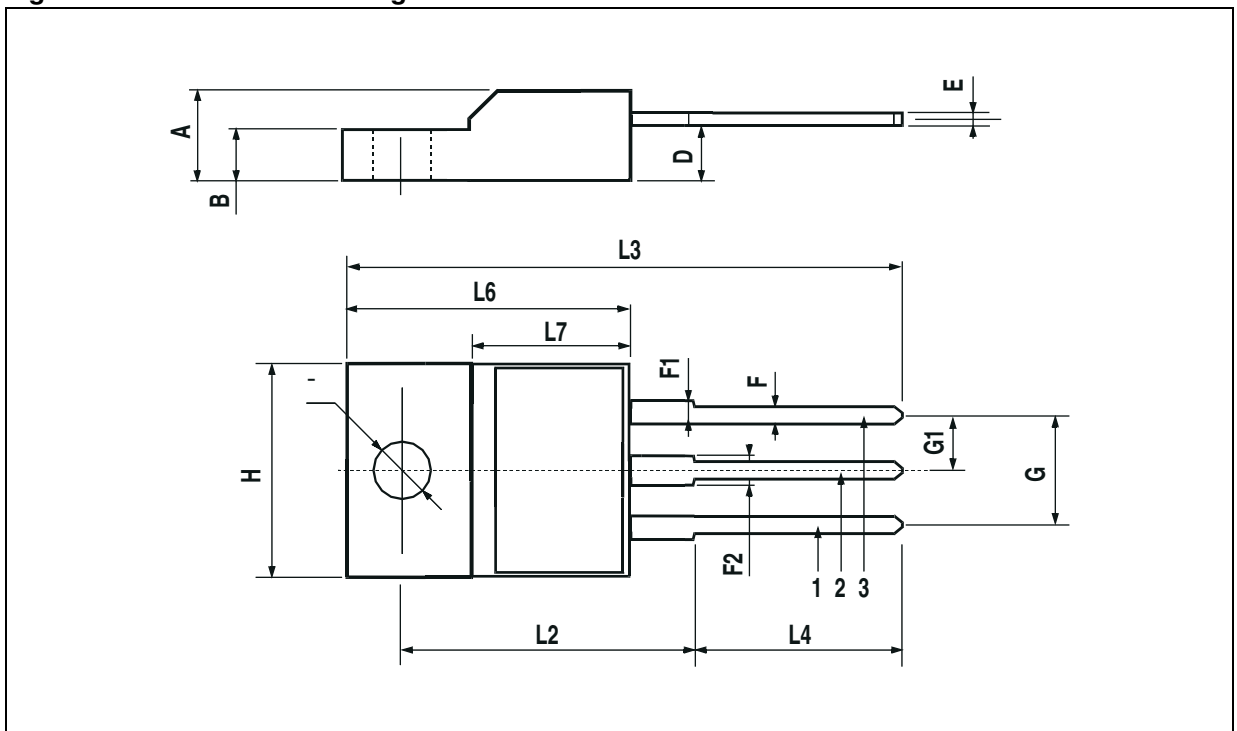
Note: Drawing is not to scale.

VND5N07/VND5N07-1/VNP5N07FI/K5N07FM

Table 13. ISOWATT220 Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.4		0.7
F	0.75		1
F1	1.15		1.7
F2	1.15		1.7
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L6	15.9		16.4
L7	9		9.3
	3		3.2

Figure 34. ISOWATT220 Package Dimensions

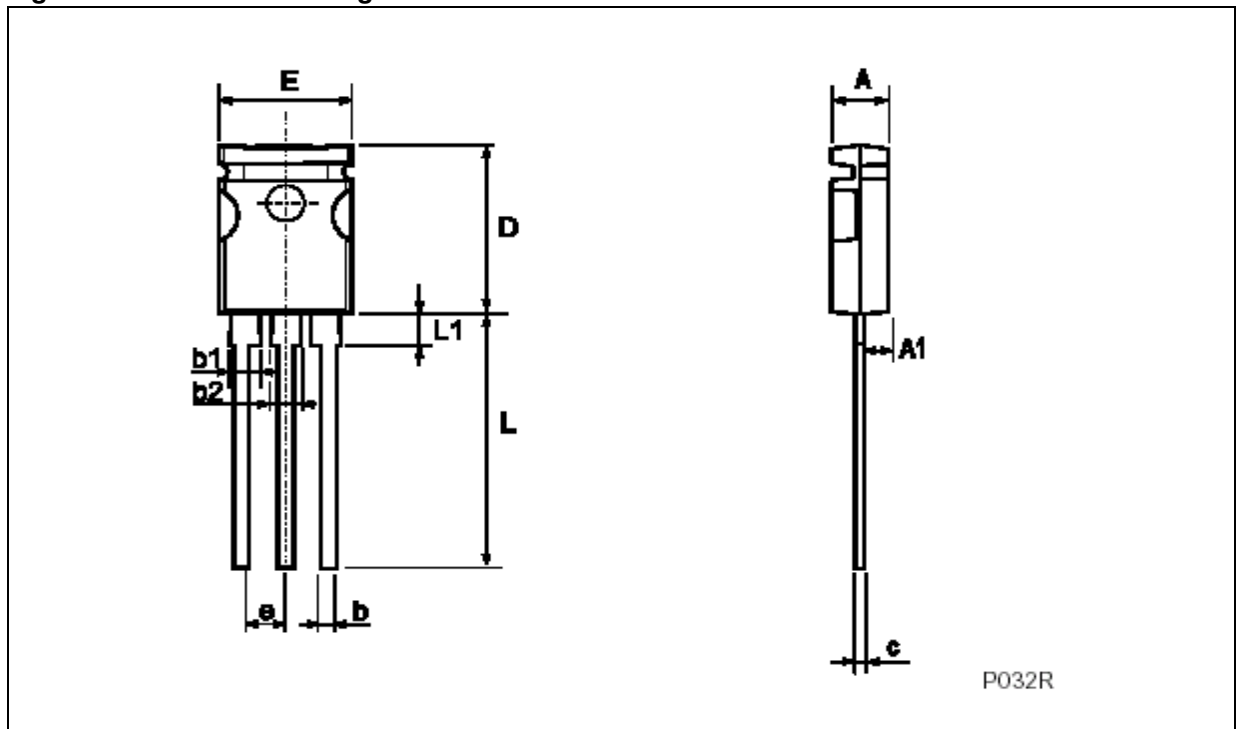


Note: Drawing is not to scale.

Table 14. SOT-82FM Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.85		3.05
A1	1.47		1.67
b	0.40		0.60
b1	1.4		1.6
b2	1.3		1.5
c	0.45		0.6
D	10.5		10.9
e	2.2		2.8
E	7.45		7.75
L	15.5		15.9
L	1 1.95		2.35

Figure 35. SOT-82FM Package Dimensions



Note: Drawing is not to scale.

**REVISION HISTORY**

**Table 15. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
June-1996	1	First Issue
18-June-2004	2	Stylesheet update. No content change.

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